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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/922,950	08/07/2001	Manabu Koga	AMA.040	9509

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EXAMINER	
DOAN, DUC T	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 06/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/922,950	KOGA, MANABU	
	Examiner	Art Unit	
	Duc T. Doan	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/19/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAIL ACTION

Status of Claims

Response to Amendment

Claims 1-18 have been presented for examination in this application. In response to the last Office Action, claims 1,3-7,9,12 have been amended. Claims 13-18 have been added. As a result, claims 1-18 are now pending in this application.

Claims 1-18 rejected.

All rejections and objections not explicitly repeated below are withdrawn.

Applicant's arguments filed 4/11/2005 have been fully considered but they are mooted in view of new ground(s) of rejection necessitated by the Applicant's amendments to the claims.

Specifications

The disclosure is objected to because of the following informalities:

Element 13 of Fig 2 is not described in the specification.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are

such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4,6-18 rejected under 35 U.S.C. 103(a) as being unpatentable over APA in view of Virajpet et al (US 6480948).

As for claim 1, APA describes a microcomputer comprising: a central processing unit (APA's Fig 1: #42); a data bus electrically connected to said central processing unit (APA's Fig 1: #43); a cache (APA's Fig 1: #47); a command bus electrically connected to said cache and separated from said data bus (APA's Fig 1: #45);

the claim further recites a memory electrically connected to said command bus, said memory storing an interruption handling routine therein; APA does not describe the claim's detail of the memory. However Virajpet describes a memory capable of storing an interrupt code (Virajpet's column 3, lines 18-26).

It would have been obvious to one of ordinary skill in the art at the time of invention to include the memory as suggested by Virajpet in APA's system to allow a quick access to the interrupt code [Thus, accesses for interrupt vectors or interrupt code will be to a relatively fast SRAM memory device instead of a relatively slower non-volatile memory device (e.g., to external ROM). Also, interrupt vector code can be changed during normal operation; Virajpet's column 3, lines 23-28].

As for claims 2-3, Virajpet describes wherein a program is written into said memory by switching memory maps when said microcomputer is turned on (Virajpet's column 4, lines 24-36]; wherein said memory is comprised of a random access memory (RAM) (Virajpet's column 4, lines 24-25).

As for claim 4, the rationale in the rejection of claim 1 is incorporated herein. APA describes first, second, third buses: a bus electrically connected to said central processing unit through a said first bus (APA's Fig 1: #48); a command cache electrically connected to said central processing unit through said second bus (APA's Fig 1: #45) and to said bus controller through a third bus (APA's Fig 1: #46);

The claim further recites a command memory electrically connected to said second bus through a said fourth bus, and for storing an interruption handling routine therein. APA does not describe the claim's detail of connecting the command memory. However, Virajpet describes the connection of the internal memory (Fig 1: #16) to the CPU (Fig 1: #10) as shown in Fig 1.

It would have been obvious to one of ordinary skill in the art at the time of invention to include the internal memory as suggested by Virajpet in APA's system to allow a direct path to the CPU, thus allowing a quick access to the interrupt code (Virajpet's column 3, lines 23-28).

As for claim 6, APA describes wherein said central processing unit, if said command cache stores a command to be executed by said central processing unit, reads said command out of said command cache, and executes the thus read-out command, and if said command cache

does not store a command to be executed by said central processing unit, reads a command out of said external memory, and executes the thus read-out command (APA's page 1, lines 27-29).

As for claims 7-12, APA does not describe the claims' detail of the command memory. However Virajpet describes as follows:

As for claim 7, Virajpet describes wherein said central processing unit reads a command out of said command memory, and executes said interruption handling routine, when interruption occurs (Virajpet's column 3, lines 17-25).

As for claim 8, Virajpet describes an external terminal electrically connected to said central processing unit (Virajpet's column 4, lines 5-11), and wherein a region in which said command memory is to be arranged is designated through said external terminal (Virajpet's column 4, lines 10-14).

As for claim 9, Virajpet describes wherein said external terminal can be operated even while said central processing unit is in operation (Virajpet's column 5, lines 17-21).

As for claim 10, Virajpet describes an external terminal electrically connected to said central processing unit, and wherein memory map are switched through said external terminal (Virajpet's column 24-35).

As for claim 11, Virajpet describes an internal register, and wherein memory maps are switched by said internal register (Virejpet's column 4, lines 36-40).

As for claim 12, Virajpet describes wherein said memory is comprised of a random access memory (RAM) (Virajpet's column 3, lines 20-25).

As for claim 13, APA describes wherein said cache comprises a command cache (Fig 1: #47).

As for claim 14, APA describes a bus adapted to be connected to an external memory storing a program to be executed by said microcomputer (Fig 1: #44).

Claim 15 rejected based on the same rationale as in claim 8.

Claim 16 rejected based on the same rationale as in claim 9.

Claim 17 rejected based on the same rationale as in claim 10.

Claim 18 rejected based on the same rationale as in claim 6.

Claim 5 rejected under 35 U.S.C. 103(a) as being unpatentable over APA in view of Virajpet et al (US 6480948) as applied to claim 4, and further in view of Ueki et al (US 6651152).

As for claim 5, APA describes a memory controller electrically connected to said bus controller through a fifth bus (APA's Fig 1: #48), to an external memory through a seventh bus

(APA's Fig 1: #50). The claim further recites to said command memory through a sixth bus (APA's Fig 1: #48). APA and Virajpet do not describe the claim's detail of connecting between the memory controller and the internal memory (corresponds to the claim's command memory). However Ueki describes a connecting (Fig 2: #28) between an external device controller (Fig 2: #50) and an sram (Fig 2: #5). It would have been obvious to one of ordinary skill in the art at the time of invention to include the connecting as suggested by Ueki in APA's system to have a direct path from the external device to the sram [The microcomputer can input/output data via DLC 50 with respect to register group 3, DRAM 4 and SRAM 5, in addition to flash memory 6; Ueki's column 2, lines 43-45].

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

Applicant's amendment filed 8/18/03 necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

When responding to the office action, Applicant is advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc T. Doan whose telephone number is 571-272-4171. The examiner can normally be reached on M-F 8:00 AM 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kevin L. Ellis
Primary Examiner